Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	Successive approximation	
Resolution	16 bits	
Number of channels	16 differential	
Input ranges (software and sequencer programmable)	Bipolar: ±10 V, ±5 V, ±2 V, ±1 V , ±0.5 V, ±0.2 V, ±0.1 V	
Maximum sample rate	1 MHz	
Nonlinearity (integral)	±2 LSB maximum	
Nonlinearity (differential)	±1 LSB maximum	
A/D pacing	Onboard input scan clock, external source (XAPCR)	
Trigger sources and modes	See [Table 7]	
Acquisition data buffer	1 MSample	
Configuration memory	Programmable I/O	
Maximum usable input voltage + common mode voltage (CMV + V_{in})	Range: ±10 V, ±5 V, ±2 V, ±1 V, ±0.5 V	10.5 V maximum
	Range: ±0.2 V, ±0.1 V	2.1 V maximum
Signal to noise and distortion	*72 dB typical for ±10 V range, 1 kHz fundamental*	
Total harmonic distortion	*-80 dB typical for ±10 V range, 1 kHz fundamental*	
Calibration	Auto-calibration, calibration factors for each range stored onboard in non-volatile RAM.	
CMRR @ 60 Hz	-70 dB typical DC to 1 kHz	
Bias current	*40 pA typical (0 °C to 35°C)*	
Crosstalk	*-75 dB typical DC to 60 Hz; -65 dB typical @ 10 kHz*	
Input impedance	*20 MΩ differential*	
Absolute maximum input voltage	*±30 V*	
Maximum usable input voltage + common mode voltage	Ranges	Maximum (CMV + V_{in})
	5, 10 V	10.5 V
	0.1, 0.2, 0.5, 1, 2 V	6.0 V

Accuracy

Table 2. Analog input accuracy specifications

Voltage range		Accuracy ±(% of reading + % range) 23°C ±10 °C, 1 year	Temperature coefficient ±(ppm of reading + ppm range)/°C	Noise (cts RMS)	
-10 V to 10 V		*0.031% + 0.008%*	*14 + 8*	2.0	
-5 V to 5 V		*0.031% + 0.009%*	*14 + 9*	3.0	
-2 V to 2 V		*0.031% + 0.010%*	*14 +10*	2.0	
-1 V to 1 V	Note 1	*0.031% + 0.02%*	*14 + 12*	3.5	Note 2
-500 mV to 500 mV		*0.031% + 0.04%*	*14 +18*	5.5	
-200 mV to 200 mV		*0.036% + 0.075%*	*14 +12*	8.0	
-100 mV to 100 mV		*0.042% + 0.15%*	*14 +18*	14.0	

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Note 1: Specifications assume single-channel scan, 1 MHz scan rate, unfiltered, CMV=0.0 V, 30 minute warm-up, exclusive of noise, range is +FS to -FS.

Note 2: Noise reflects 10,000 samples at 1 MHz, typical, differential short.

Analog outputs

Analog output channels can be updated synchronously relative to scanned inputs, and clocked from either an internal onboard clock, or an external clock source. Analog outputs can also be updated asynchronously, independent of any other scanning system.

Table 3. Analog output specifications

Channels	2
Resolution	16-bits
Data buffer	PC-based memory
Output voltage range	±10 V
Output current	±1 mA
Offset error	±0.0045 V maximum
Digital feed-through	<10 mV when updated
DAC analog glitch	<12 mV typical at major carry
Gain error	±0.01%
Coupling	DC
Update rate	1 MHz maximum, resolution 20.83 ns
Settling time	2 μs to rated accuracy, 10 V step.
Pacer sources	Three programmable sources: ▪ Onboard output scan clock, independent of input scan clock ▪ Onboard input scan clock ▪ External input scan clock (XAPCR)
Trigger sources	Start of input scan

Digital input/output

Table 4. Digital input/output specifications

Number of I/O	16
Ports	Two banks of eight. Each port is programmable as input or output
Input scanning modes	Two programmable ▪ Asynchronous, under program control at any time relative to input scanning ▪ Synchronous with input scanning
Input characteristics	220 Ω series resistors, 20 pF to common
Logic keeper circuit	Holds the logic value to 0 or 1 when there is no external driver
Input protection	±15 kV ESD clamp diodes parallel
Input high	*+2.0 V to +5.0 V*
Input low	*0 to 0.8 V*
Output high	*>2.0 V*
Output low	*<0.8 V*
Output current	Output 1.0 mA per pin
Digital input pacing	Onboard input scan clock, external input scan clock (XAPCR)
Digital output pacing	Three programmable sources: ▪ Onboard output scan clock, independent of input scan clock ▪ Onboard input scan clock ▪ External input scan clock (XAPCR)

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Digital input trigger sources and modes	See Table 7
Digital output trigger sources	Start of input scan
Sampling/update rate	4 MHz maximum (rates up to 12 MHz are sustainable on some platforms)
Pattern generation output	Both 8-bit ports can be configured to support 16-bit pattern generation. The pattern can also be updated synchronously with an acquisition at up to 4 MHz.

Counters

Counter inputs can be scanned based on an internal programmable timer or an external clock source.

Table 5. Counter specifications

Channels	4 independent
Resolution	32-bit
Input frequency	20 MHz maximum
Input signal range	-5 V to 10 V
Input characteristics	10 kΩ pull-up, 200 Ω series resistor, ±15 kV ESD protection
Trigger level	TTL
Minimum pulse width	25 ns high, 25 ns low
Debounce times	16 selections from 500 ns to 25.5 ms, positive or negative edge sensitive, glitch detect mode or debounce mode
Time base accuracy	50 ppm (0 ° to 50 °C)
Counter read pacer	Onboard input scan clock, external input scan clock (XAPCR)
Trigger sources and modes	See Table 7
Programmable mode	Counter
Counter mode options	Totalize, clear on read, rollover, stop at all Fs, 16- or 32-bit, any other channel can gate the counter

Input sequencer

Analog, digital, and counter inputs can be scanned based on either an internal programmable timer or an external clock source.

Table 6. Input sequencer specifications

Input scan clock sources: two (see Note 3)	Internal, programmable: ▪ Analog channels from 1 µs to 1 s in 20.83 ns steps. ▪ Digital channels and counters from 250 ns to 1 s in 20.83 ns steps. External. TTL level input (XAPCR): ▪ Analog channels down to 1 µs minimum ▪ Digital channels and counters down to 250 ns minimum
Programmable parameters per scan	Programmable channels (random order), programmable gain
Depth	512 locations
Onboard channel-to-channel scan rate	Analog: 1 MHz maximum Digital: 4 MHz if no analog channels are enabled, 1 MHz with analog channels enabled
External input scan clock (XAPCR) maximum rate	Analog: 1.0 MHz Digital: 4 MHz if no analog channels are enabled, 1 MHz with analog channels enabled
Clock signal range:	Logical zero: 0 V to 0.8 V Logical one: 2.4 V to 5.0 V
Minimum pulse width	50 ns high, 50 ns low

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Note 3: The maximum scan clock rate is the inverse of the minimum scan period. The minimum scan period is equal to 1 μs times the number of analog channels. If a scan contains only digital channels, then the minimum scan period is 250 ns.

Some platforms can sustain clock rates up to 83.33 ns.

External acquisition scan clock

Pin name	XAPCR
Pin type	Bidirectional
Input	Maximum rate ▪ Analog: 990 kHz ▪ Digital: 4 MHz if no analog channels are enabled, 1 MHz with analog channels enabled
	Clock input signal range: ▪ Logical zero: 0 V to 1.0 V ▪ Logical one: 2.3 V to 5.0 V Input pulled up to +3.3 V through 2.47 kΩ
	Minimum pulse width: 50 ns high, 50 ns low
Output	Clock output signal range: ▪ Logical one: 137 Ω to +3.3 V ▪ Logical zero: 130 Ω to ground
	Output pulse width: 42 ns high, occurs on every rising edge of the internal pacer clock.

Triggering

Table 7. Trigger sources and modes

Trigger source	Explanation
Single channel analog hardware trigger	Any analog input channel can be software programmed as the analog trigger channel, including any of the analog expansion channels. ▪ Input signal range: -10 V to +10 V maximum ▪ Trigger level: Programmable (12-bit resolution) ▪ Latency: 350 ns typical, 1.3 μs max ▪ Accuracy: ±0.5% of reading, ±2 mV offset maximum ▪ Noise: 2 mV RMS typical
Single channel analog software trigger	Any analog input channel can be selected as the software trigger channel. ▪ Input signal range: Anywhere within range of the trigger channel ▪ Trigger level: Programmable (16-bit resolution) ▪ Latency: One scan period (maximum)
Single channel digital trigger	A separate digital input is provided for digital triggering (TTLTRG). ▪ Input signal range: -15 V to +15 V maximum ▪ Trigger level: TTL level sensitive ▪ Minimum pulse width: 50 ns high, 50 ns low ▪ Latency: One scan period maximum
Digital pattern triggering	8-bit or 16-bit pattern triggering on any of the digital ports. Programmable for trigger on equal, not equal, above, or below a value. ▪ Individual bits can be masked for "don't care" condition. ▪ Latency: One scan period, maximum
Counter/totalizer triggering	Counter/totalizer inputs can trigger an acquisition. User can select to trigger on a frequency or on total counts that are equal, not equal, above, or below a value, or within/outside of a window rising/falling edge. ▪ Latency: One scan period, maximum

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Frequency/pulse generators

Table 8. Frequency/pulse generator specifications

Channels	2 × 16-bit
Output waveform	Square wave
Output rate	1 MHz base rate divided by 1 to 65535 (programmable)
High-level output voltage	2.0 V minimum @ -1.0 mA, 2.9 V minimum @ -400 µA
Low-level output voltage	0.4 V maximum @ 400 µA

Power consumption

Table 9. Power consumption specifications

Power consumption (per board)	2.5 W maximum

External power

The power supply (MCC p/n TR-2U) and line cord (MCC p/n CA-1) are required.

Table 10. External power specifications

Connector	Switchcraft # RAPC-712
Power range	6 to 16 VDC
Over-voltage	20 V for 10 seconds, maximum

USB specifications

Table 11. USB specifications

USB-device type	USB 2.0 high-speed mode (480 Mbps) if available (recommended), otherwise, USB1.1 full-speed mode (12 Mbps)
Device compatibility	USB 2.0 (recommended) or USB 1.1

Environmental

Table 12. Environmental specifications

Operating temperature range	-30 °C to +70 °C
Storage temperature range	-40 °C to +80 °C
Relative humidity	0 to 95% non-condensing

Mechanical

Table 13. Mechanical specifications

Vibration	MIL STD 810E category 1 and 10
Dimensions	280 mm W x 216 mm D x 45 mm H (11.0" x 8.5 x 1.75")
Weight	1.39 kg (3.06 lbs)

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Signal I/O connectors and pin out

Table 14. Screw connector specifications

Connector type	▪ Analog inputs: 16 standard BNC female connectors for analog input. Center conductor is high (+), shell is low (-). ▪ DIO, AO,CTR, Timer: 37-pin DSUB (See Table 15)
Compatible cables	C37FM-*x* (*x* = length in feet)
Compatible accessories	▪ SCB-37 ▪ CIO-MINI37 ▪ CIO-MINI37-VERT ▪ CIO-TERMINAL

Table 15. USB-1616HS-BNC 37-pin DSUB connector pin out

Pin number	Name	Description
1	SELFCAL	Self-calibration. Factory use only. Do not connect.
2	DAC0	Digital-to-analog converter; analog output 0
3	AGND	Analog common
4	TMR1	Timer output 1; 16-bit, frequency pulse generator output
5	DGND	Digital common
6	TMR0	Timer output 0; 16-bit, frequency pulse generator output
7	TTLTRG	TTL trigger input
8	CTR2	Counter input, CTR2
9	CTR0	Counter input, CTR0
10	Port B – B0	Digital I/O: digital port B, bit 0
11	Port B – B2	Digital I/O: digital port B, bit 2
12	Port B – B4	Digital I/O: digital port B, bit 4
13	Port B – B6	Digital I/O: digital port B, bit 6
14	DGND	Digital common
15	Port A – A0	Digital I/O: digital port A, bit 0
16	Port A – A2	Digital I/O: digital port A, bit 2
17	Port A – A4	Digital I/O: digital port A, bit 4
18	Port A – A6	Digital I/O: digital port A, bit 6
19	DGND	Digital common
20	SGND	Signal Ground
21	DAC1	Digital to analog converter; analog output 1
22	AGND	Analog common
23	+5VDC	+5 VDC power out
24	XPACR	A/D Pacer clock I/O
25	DGND	Digital common
26	CTR3	Counter input, CTR3
27	CTR1	Counter input, CTR1
28	DGND	Digital common
29	Port B – B1	Digital I/O: digital port B, bit 1
30	Port B – B3	Digital I/O: digital port B, bit 3
31	Port B – B5	Digital I/O: digital port B, bit 5
32	Port B – B7	Digital I/O: digital port B, bit 7
33	DGND	Digital common
34	Port A – A1	Digital I/O: digital port A, bit 1
35	Port A – A3	Digital I/O: digital port A, bit 3
36	Port A – A5	Digital I/O: digital port A, bit 5
37	Port A – A7	Digital I/O: digital port A, bit 7

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